Power Loss Estimation in a Modular Multilevel Rectifier

1st Anita Mijajlović
School of Electrical Engineering, University of Belgrade
Belgrade, Serbia
ma243020m@student.etf.bg.ac.rs

2nd Francisco De Paula García López
Department of Electrical Engineering, University of Seville
Seville, Spain
fdpgarcia@us.es

3rd Milovan Majstorović
School of Electrical Engineering, University of Belgrade
Belgrade, Serbia
majstorovic@etf.bg.ac.rs

4th Manuel Barragán-Villarejo
Department of Electrical Engineering, University of Seville
Seville, Spain
manuelbarragan@us.es

5th Bogdan Brković
School of Electrical Engineering, University of Belgrade
Belgrade, Serbia
brkovic@etf.bg.ac.rs

6th José María Maza-Ortega
Department of Electrical Engineering, University of Seville
Seville, Spain
jmmaza@us.es

7th Leposava Ristić
School of Electrical Engineering, University of Belgrade
Belgrade, Serbia
leposava.ristic@etf.bg.ac.rs

***Abstract*—This paper investigates the power losses of the Modular Multilevel Rectifier (MMR), a topology increasingly used in high and medium voltage applications. While MMRs are well-studied in terms of design and control, limited research has focused on their loss calculation and efficiency. An analytical model for loss calculation is proposed, utilizing manufacturer-provided switching component data. The model's accuracy is verified through comparison with results obtained from PLECS software. Understanding power losses in MMRs is crucial for their broader adoption, contributing to more cost-effective and scalable implementations.**

***Index Terms*—MMR, loss calculation, analytical model, PLECS**

I. Introduction

Rapid advancements in fields that rely on high-power converters demand more sophisticated solutions than conventional approaches. This creates opportunities for the broader adoption of Modular Multilevel Converters (MMCs) due to their modular construction, voltage scalability, and high power quality [1]. An MMC, which belongs to the class of voltage-source converters, consists of identical submodules (SMs) connected in a cascaded configuration, enabling uniform voltage distribution. This topology effectively addresses the challenges associated with sizing semiconductor components in high-power applications, where the cost-effectiveness of MMCs becomes particularly evident [2]. The MMR is essentially an adaptation of the MMC, focusing specifically on the rectification function. While the MMC is versatile and capable of performing both AC–DC and DC–AC conversions, the MMR retains the modular structure and advantages of the MMC while being optimized for rectification.

Medium-voltage DC (MVDC) has the potential to replace AC in various applications due to its superior transmission capacity, increased flexibility, and improved controllability [3]. The MMR provides a stable DC output with high efficiency and reliability, making it suitable for MVDC systems, where MMRs are widely adopted to enhance grid stability, manage power flows and transmit energy generated by offshore wind farms [4]. The MMR may alternatively serve as AC-DC conversion stage in MMC-based motor drive. The MMRs are also a preferred choice in High-voltage DC (HVDC) systems. For instance, they are used as the first stage in back-to-back converter configurations within HVDC installations that interconnect two asynchronous AC systems over long distances [5]. Additionally, the MMR is commonly used in applications such as electrolysis and DC-powered datacenters [6].

Efficiency is a critical parameter in MMR applications, where even minor improvements can be highly beneficial. Power losses influence thermal performance and cooling system design, directly affecting the converter's complexity and overall mass. Although MMRs are well-researched in terms of design and control, studies on loss evaluation and efficiency remain limited. This paper aims to address this gap.

The paper is organized as follows: Section II provides a

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brief overview of the operating principle, modeling and control technique of MMR, while Section III focuses on the power loss estimation model. Section IV presents the results of the proposed model and their verification, followed by conclusions and future research directions in Section V.

II. Operating Principle, Modeling, and Basic Control Techniques

The topology of MMR is illustrated in Figure 1. The AC input terminal is positioned at the midpoint of the leg, dividing it into an upper and a lower arm. Each arm contains *N* SMs. The Half-Bridge submodule topology is considered, as it is the most widely used configuration due to its simplicity in both construction and control [7]. Each submodule comprises two switches, Q_1 and Q_2. The analysis focuses on IGBTs, which are commonly used as controllable switching elements in modular topologies. Diodes D_1 and D_2 represent the free-wheeling diodes associated with the IGBTs. The parameters L_{arm} and *r* represent the inductance and resistance of the arm, respectively, while the load is of a resistive (*R*) nature.

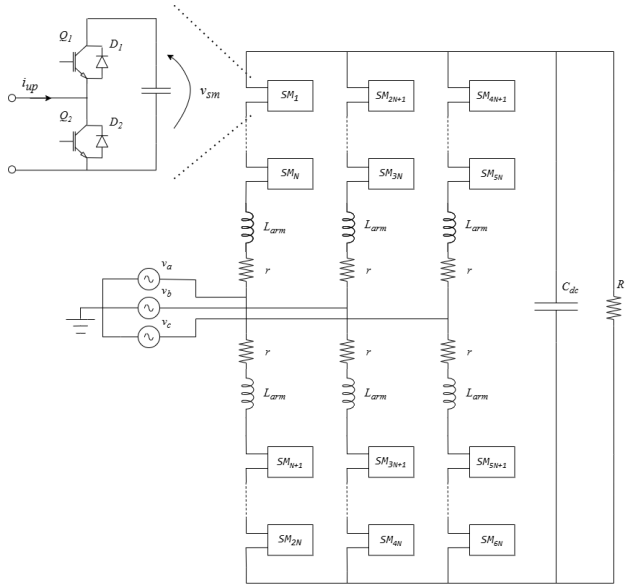


Fig. 1: Three-phase MMR topology

A. Voltage Modulation

A total of N SMs per arm enables the generation of $N+1$ distinct voltage levels within the arm, ranging from 0 to Nv_{sm}. When the upper switch is turned on, the submodule's output voltage equals (assuming ideal switches) the capacitor voltage (v_{sm}), in which case the submodule is said to be inserted. Conversely, if the lower switch is turned on, the output voltage of the submodule is zero, indicating that the submodule is bypassed. Pulse Width Modulation (PWM) is the most widely used technique for controlling multilevel topologies. In the Level-Shifted Carrier PWM (LSC-PWM) scheme, triangular carrier signals of equal amplitude are disposed vertically. However, this method is generally less preferred due to its tendency to produce an uneven distribution of power losses among the submodules [8]. This paper investigates the power loss characteristics of the LSC-PWM strategy, focusing on the non-uniform conduction among submodules. The analysis is conducted using the Phase-Displaced technique, in which the triangular carrier signals are vertically aligned and in-phase with one another.

B. Control algorithm

Figure 2 presents the control block diagram adopted for the simulation purposes.

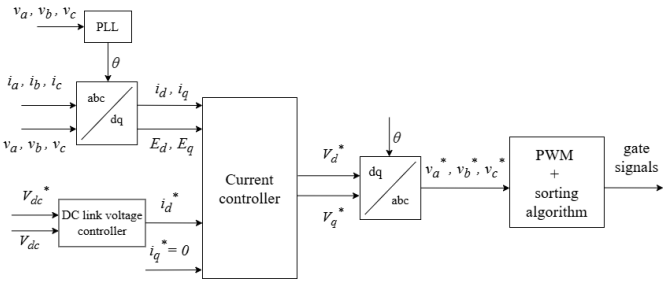


Fig. 2: Control block diagram of MMR

The grid voltage is used to feed the Phase-Locked Loop (PLL), and the calculated voltage angle is then employed for the transformation of the three-phase line current and voltage into the dq-coordinate system. Subsequently, the dq-coordinate values (i_d, i_q, E_d, E_q), along with the DC-link voltage (V_{dc}), are fed into a decoupled controller (DC link voltage controller and Current controller) implemented using PI regulators [9]. The reference current for the d-component is derived from the DC-link voltage controller, based on the required active power. The unit power factor (UPF) condition is achieved when the line current vector is aligned with the line voltage vector, which corresponds to setting the i_q reference to zero. Finally, the reference voltages generated by the controller are transmitted to the PWM block, where switching patterns are created according to the implemented sorting algorithm. The sorted submodules are then modulated using LSC-PWM strategy.

III. Power loss estimation model

A converter with six SMs per arm is analyzed for the purpose of both the analytical loss calculation and the PLECS simulation used to validate the obtained results. The converter parameters are provided in Table I.

TABLE I: Three-phase MMR parameters

Parameter	Symbol	Value
DC-link voltage	V_{dc}	3050 V
Grid phase RMS voltage	$v_{a,b,c}$	1000 V
DC link capacitance	C_{dc}	1 mF
Load	R	312.5 Ω
Switching frequency	f_{sw}	6 kHz
Fundamental frequency	f	50 Hz
Number of submodules per arm	N	6
Dead time	t_d	2 μs

From the perspective of power loss calculation, it is important to emphasize that the simulation includes dead-time (t_d) effects and that the freewheeling diodes of the IGBTs are modeled separately, rather than being integrated within the switch models themselves. In the subsequent sections, the methodology for modeling power losses in PLECS will be outlined, and the model based on manufacturer data for switching components (analytical model) will be presented, after which a comparison of the results will be conducted. Loss evaluation was carried out using the switching device identified by Mfr. No. IKP15N60T.

A. Power loss modeling in the PLECS software

Considerable number of manufacturers provide PLECS thermal models of switching components, enabling loss calculations within the PLECS software environment using imported models and pre-configured blocks. The software performs these calculations based on lookup tables embedded within the models. Since the data in these tables are temperature-dependent, it is necessary to place the components on an isothermal surface (heat sink), whose thermal properties, such as initial temperature and thermal capacitance, can be configured. Heat exchange occurs between components in contact with the isothermal surface, which causes variations in its temperature. To simplify the analysis, the calculation was carried out assuming a constant temperature of heat sink throughout the converter's operation.

1) Conduction power loss modeling: Conduction power losses are modeled in PLECS using a Periodic Average block. This block is employed to average the input signal over a specified period. Conduction losses fluctuate throughout the switching periods due to variations in current. However, it is expected that after one fundamental current period, the time-dependent pattern of conduction losses will repeat. Therefore, the averaging within this block is configured to occur over a 20 ms interval.

2) Switching power loss modeling: For the calculation of switching losses, the Periodic Impulse Average block is used to average Dirac pulses over a specified period, as switching losses in PLECS are represented as pulses. The block updates its output at the end of each specified period. The pulse averaging period is set to match the commutation period, $1/f_{sw}$. The resulting values are then averaged with a 20 ms period within the Periodic Average block for comparison with the analytical model presented in the following section.

B. Analytical power loss model

The specifications provided by manufacturers contain all the necessary data for performing analytical calculations of conduction and switching losses in power semiconductor devices under various operating conditions (e.g., different voltage, current, and temperature levels). These calculations are based on the utilization of voltage and current waveforms obtained from PLECS simulations conducted with idealized switching components.

1) Analytical conduction power loss modeling: The application of the previously explained control algorithm ensures that, in each leg, N submodules are inserted and N submodules are bypassed at all times. The only exception to this condition occurs during the dead time, as the submodule is neither inserted nor bypassed, but conducts through the freewheeling diode. The dead time period begins after the turn-off of one switch and lasts until the turn-on of the other, in order to prevent both switches from conducting simultaneously. The calculation was first performed for the upper arm of phase A and is applicable to any other arm, using the corresponding waveforms. For the purpose of the calculation, it can be reasonably assumed that the current does not vary significantly over a single switching period. Therefore, the average arm current value within the switching period $T_{sw,i}$ is used ($\langle i_{up}\rangle_{T_{sw,i}}$). Accordingly, a variable *n* is defined to represent number of switching cycles that occur within a single fundamental period of the signal, which in this case is:

$$n = \frac{f_{sw}}{f} = 120 \tag{1}$$

Since the IGBT conducts current from the collector to the emitter, while reverse current is conducted by the anti-parallel freewheeling diode, the method for calculating power losses depends on the direction of the arm current and requires information on the number of inserted submodules. The number of inserted submodules in the upper arm during the switching period $T_{sw,i}$ is defined as a function of the average value of the phase A reference AC voltage ($\langle v_a^*\rangle_{T_{sw,i}}$) over that switching period, and can be expressed as:

$$\langle n\rangle_{T_{sw,i}} = \left(\frac{1}{2} - \frac{\langle v_a^*\rangle_{T_{sw,i}}}{V_{dc}}\right) N,\ i \in [1, n] \tag{2}$$

For the positive current direction in the arm with inserted submodules ($i_{up} > 0$), the freewheeling diode D_1 conducts, while for bypassed submodules, the switch Q_2 conducts, as indicated by the labels in Figure 1. Of the n elements in the current array, n_p corresponds to the positive elements, and n_n corresponds to the negative ones, such that the following holds:

$$n = n_p + n_n \tag{3}$$

The elements of the conduction loss matrix corresponding to the positive current direction ($j \in [1, n_p]$) are calculated using the following expression:

$$\begin{aligned} P_{cond}^{pos}(j) = \langle n\rangle_{T_{sw,j}}(V_{FD} + r_{FD}\langle i_{up}\rangle_{T_{sw,j}}) \cdot \langle i_{up}\rangle_{T_{sw,j}} + \\ +(N - \langle n\rangle_{T_{sw,j}})(V_{FQ} + r_{FQ}\langle i_{up}\rangle_{T_{sw,j}}) \cdot \langle i_{up}\rangle_{T_{sw,j}}, \end{aligned} \tag{4}$$

where V_{FD}, r_{FD}, V_{FQ} and r_{FQ} represent the conduction

characteristics of the freewheeling diode and the switch, respectively, and are dependent on temperature and gate-emitter voltage.
For negative current values ($k \in [1, n_n]$), conduction occurs through switch Q_1 in the inserted submodules and through diode D_2 in the bypassed submodules. As a result, the equation for calculating conduction losses takes the following form:

$$P_{cond}^{neg}(k) = \langle n \rangle_{T_{sw,k}} (V_{FQ} + r_{FQ} |\langle i_{up} \rangle_{T_{sw,k}}|) \cdot |\langle i_{up} \rangle_{T_{sw,k}}| + \\ + (N - \langle n \rangle_{T_{sw,k}})(V_{FD} + r_{FD} |\langle i_{up} \rangle_{T_{sw,k}}|) \cdot |\langle i_{up} \rangle_{T_{sw,k}}| \tag{5}$$

To the previously obtained average value of the matrix composed of P_{cond}^{pos} and P_{cond}^{neg} elements it is necessary to add the conduction losses of the reverse diodes occurring during the dead time:

$$P_{deadtime}^{IGBT} = \frac{\sum_{i=1}^{n} (V_{FD} + r_{FD} |\langle i_{up} \rangle_{T_{swi}}|) \cdot |\langle i_{up} \rangle_{T_{swi}}|}{n} f_{sw} t_d \tag{6}$$

2) Analytical switching power loss modeling: Device manufacturers typically provide energy loss data per switching event under specified conditions, including the turn-on energy (E_{on}) and turn-off energy (E_{off}) for the IGBT, as well as the reverse recovery energy (E_{rr}) for the diode.
The implementation of the previously discussed control algorithm ensures that, within a single switching period, the submodule state transitions occur twice. For the reference current direction of the arm, as illustrated in Figure 1, the switching events within a single switching period, followed by their associated energy losses can be summarized as follows:

Inserted → Bypassed :

$i_{up} > 0$: D_1 Turn ON → 0
Q_2 Turn OFF → E_{off}

$i_{up} < 0$: Q_1 Turn ON → E_{on}
D_2 Turn OFF → E_{rr}

Bypassed → Inserted :

$i_{up} > 0$: D_1 Turn OFF → E_{rr}
Q_2 Turn ON → E_{on}

$i_{up} < 0$: Q_1 Turn OFF → E_{off}
D_2 Turn ON → 0

It can be concluded that, irrespective of the current direction, the energy losses during a single switching period of the submodule can be expressed with (7).

$$E_{comm} = E_{on} + E_{off} + E_{rr} \tag{7}$$

It is important to understand the influence of the reverse-recovery effect in diodes, which will first be illustrated through the Double Pulse Test topology shown in Figure 3 [10].
Figure 4 reveals five distinct characteristic regions obtained from the analysis of the turn-on process of switch Q within

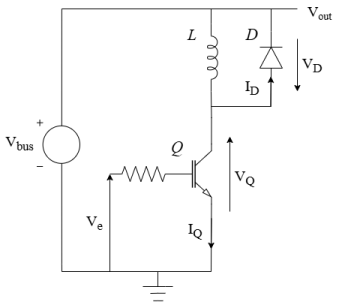


Fig. 3: Double Pulse Test topology

the submodule, which is preceded by conduction through diode D, as denoted in Figure 3. This scenario corresponds to the turn-on of the switch following the dead time interval, during which the diode of the complementary switch conducts. The following regions can be identified:

- 1 and 2: Switching losses resulting from the increase in the switch current during turn-on.
- 3: Losses associated with the voltage variation during turn-on, independent of the diode behavior.
- 4: Losses due to extended commutation time, influenced by the diode's reverse recovery.
- 5: Losses that are intrinsic to the switch and would occur even in the case of an ideal diode.

Therefore, the diode reverse recovery current not only causes turn-off losses in the diode, but also contributes to an increase in the turn-on current of the switch and extends the turn-on duration, resulting in additional losses in the switch. Accordingly, it is essential to assess whether the turn-on energy (E_{on}) provided in the manufacturer's datasheet accounts for the losses associated with the reverse recovery of the diode.

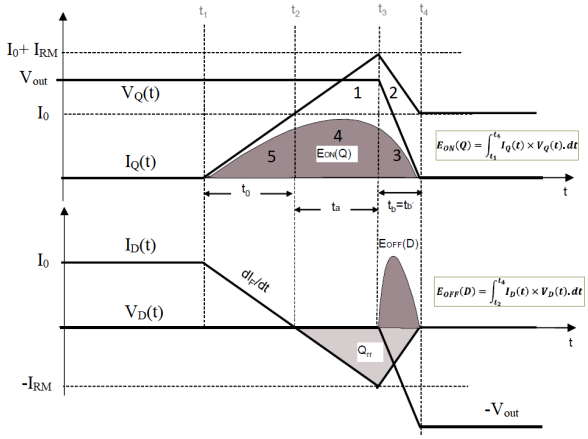


Fig. 4: Ideal waveforms during Q turn-on and D turn-off

Eventually, the switching power losses for arm averaged over a 20 ms interval can be determined using the following expression:

$$P_{comm} = N \cdot (E_{on} + E_{off} + E_{rr}) \cdot f \cdot n_{comm}, \tag{8}$$

where n_{comm} denotes the average number of submodule commutations per leg within a 20 ms interval. Considering that the total switching frequency per arm is 6 kHz and that each arm comprises 6 submodules, the corresponding switching frequency per submodule is 1 kHz. Therefore, 20 switching periods are expected within a 20 ms interval. However, simulation results indicate that $n_{comm} \approx 40$, as shown in Figure 5. This increase is attributed to the capacitor voltage balancing mechanism within the submodules, which effectively doubles the switching frequency.

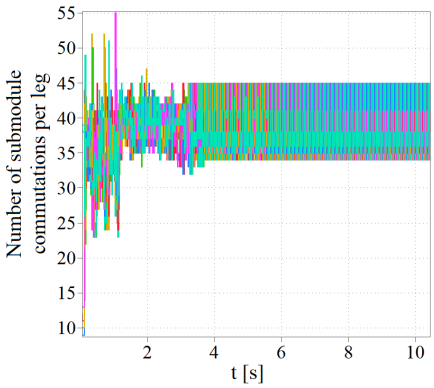


Fig. 5: Number of submodule commutations

The values of E_{on}, E_{off} and E_{rr} were obtained through Double Pulse Testing of the selected switch.

IV. Verification of the Analythical Model

The operation of the converter was simulated using the PLECS software, based on the parameter values provided in Table I. Figure 6 shows the waveform of the output voltage, with the voltage ramp reference applied at $t = 2$ s of the simulation. Figure 7 illustrates the upper arm current of phase A (a) alongside the voltage of phase A (b).

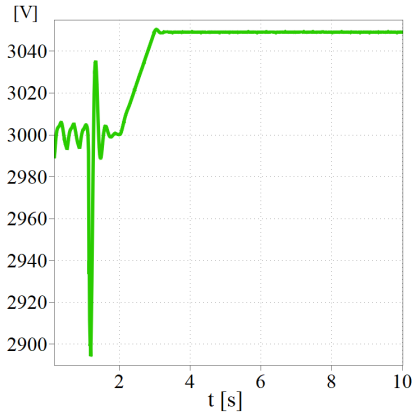
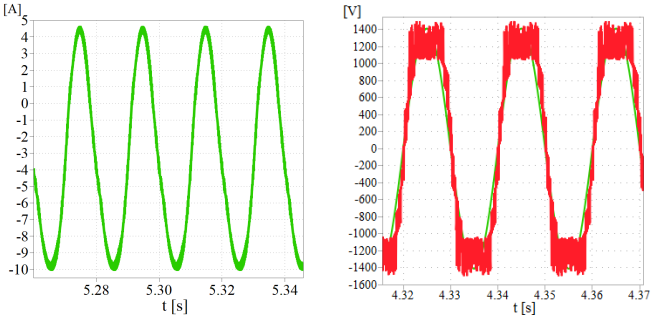


Fig. 6: DC-link voltage

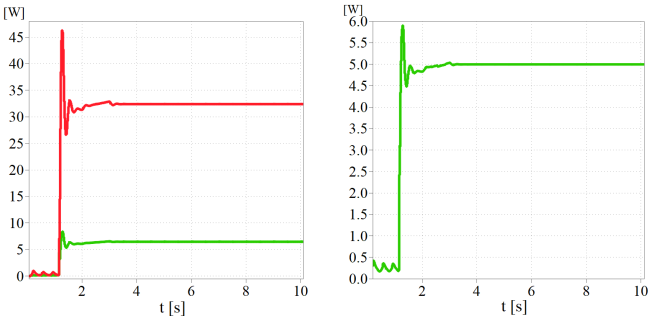
The losses dissipated by the switching components in the described modular multi-level converter were determined using two methods: first, through simulation in PLECS, with the



(a) Phase A upper arm current (b) Phase A voltage

Fig. 7: Phase A waveforms

results presented in Figure 8, and second, through analytical calculations based on manufacturer-provided data. In Figure 8 (a), the conduction losses in the diodes of the arm are indicated in red, while the conduction losses in the switches of the arm are shown in green. Figure 8 (b) illustrates the obtained switching losses in the arm, which are, as expected, significantly lower than the conduction losses.



(a) Conduction power losses (b) Switching power losses

Fig. 8: Power losses obtained from PLECS simulation

The results of the analytical model are compared with the corresponding PLECS simulation results in Table II. The close agreement with simulation outcomes, as evidenced by the small deviations, suggests that the analytical model is appropriately developed and reliably captures the dominant loss mechanisms.

TABLE II: Loss calculation results

Power loss [W]	PLECS	Analytical model	Deviation [%]
Conduction per arm	38.863	37.286	-4.229
Switching per arm	5.276	5.723	7.811
Total in MMR	264.834	258.054	-2.627

The slight discrepancies in conduction losses can be attributed to uncertainties in extracting data from manufacturer datasheet graphs. Switching losses, represented by the energies E_{on}, E_{off}, and E_{rr}, depend on the voltage at which the switch is turned on. In PLECS simulations, the gate signal is modeled as a logical high or low, making the exact evaluation voltage uncertain, whereas the Double Pulse Test requires explicit turn-on and turn-off voltages, which may not precisely match

the simulation conditions and can lead to differences in the calculated switching losses.

While this study evaluated losses in rectification mode, the same methodology applies to inverter operation, where the altered DC component of the arm currents results in higher RMS values and consequently increased conduction losses, as demonstrated in [11].

V. Conclusion

This paper presents an analysis of power losses in MMR, introducing two simplified methods. The analytical model offers an advantage over PLECS simulations with thermal component models for loss estimation across different operating conditions. It requires data collection from the manufacturer's catalog only once and uses ideal switch simulations, thereby significantly reducing the simulation time. It is also beneficial because it enables loss calculation for components lacking thermal models. Comparative analysis with results obtained from PLECS simulations has demonstrated that the proposed analytical model provides a high degree of accuracy, validating its suitability for practical loss estimation. Future research should include a comparative analysis with conventional topologies, such as two-level converters employing transformers, to better assess the advantages and application potential of modular multilevel structures.

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